Monolithic Supply Modulated RF Power Amplifier and DC-DC Power Converter IC

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Abstract - Mobile communication systems require highly efficient, linear, and integrated power amplifiers. This paper reports the results of a monolithic envelope following system implemented in a 0.18μm *SiGe BiCMOS* process technology. The monolithic envelope following system consists of a synchronous buck *DC-DC* converter, which is integrated with and provides the power supply for a 900 MHz power amplifier while tracking the envelope of the *RF* input signal.

I. INTRODUCTION

For state-of-the-art mobile terminals, a multi-output centralized power management unit powers various sections of the mixed signal *IC*s, memory chips, *RF* front-end, synthesizers, digital base-band, signal processors, and micro-controller through *I/O* pads and interconnects. Technology trend is toward combining these functional blocks and ideally generating a system on a chip (SOC) solution. As these *IC*s are scaled to deep sub-micron dimensions internal switching frequencies become orders of magnitude faster than off-chip signals. In this case external power supplies and control logic are incapable of responding to varying load conditions without significant delay. Another problem is the mixed-signal coupling, where the power bus lead inductance causes ground and V_{dd} bounce caused by the digital switching noise. This will generate switching noise on the power lines connected to sensitive analog and RF sections. Significant reduction in power supply interconnect delay can be achieved by proper placement of on-chip *DC-DC* converters in proximity of circuit blocks, as is shown in Fig. 1. Elimination of *I/O* pads and closer location to the load reduces the resistive losses and the inductance in the path, which improves the converter transient response. As a result, the sensitive blocks of the chip are isolated from other less sensitive ones and the multiple-level distribution networks are replaced with a single power bus while maintaining the required multiple level outputs.

Power amplifiers (*PA*'s) typically dominate the power consumption of portable wireless handsets. Therefore efficient radio frequency (*RF*) *PA*'s are highly desirable to extend the battery operation. The behavior of a *PA* is determined by its conduction angle, input signal overdrive, and output load impedance. Depending on its conduction angle and input signal overdrive, *PA* can operate in any one of the classical modes. There is an inherent tradeoff between linearity and efficiency in the amplifier design. For modulation schemes such as *QPSK* or multi-carrier signaling *PA*'s usually operate with large peak to average power ratios to allow for the required variation of *RF* signal envelopes. Amplifiers typically operate in class-A or class-AB to minimize distortion, however for linear operation modes *PA*'s operate at less than their maximum output power resulting in reduced power efficiency. Several techniques have been reported to improve the *PA* efficiency. In order to increase the *PA* efficiency without compromising the output power, the gate drive can be increased until the transistor operates as a switch. A switched-mode *PA* can be highly efficient but will also be highly non-linear. Envelope elimination and restoration (*EER*) [1] is a well-known technique, which linearizes the switched-mode *PA* without compromising its efficiency. The *RF* input signal, $v_{in}(t)$, with envelope $A_{in}(t)$ and phase $\varphi_{in}(t)$ is applied to a limiter, which eliminates $A_{in}(t)$ and generates a constant amplitude phase signal. An envelope detector extracts the magnitude information $A_{in}(t)$ from $v_{in}(t)$ and finally an efficient switched-mode *RF PA* recombines the magnitude and phase information to restore the desired *RF* output signal $v_{out}(t)$.

$$v_{in}(t) = A_{in}(t)\cos(\omega_{RF}t + \phi_{in}(t)) \quad (1)$$

$$v_{out}(t) = A_{out}(t)\cos(\omega_{RF}t + \phi_{out}(t)) \quad (2)$$

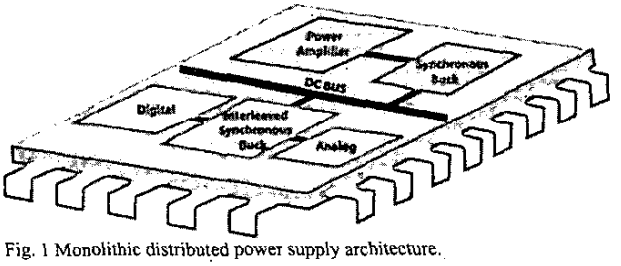

Fig. 1 Monolithic distributed power supply architecture.

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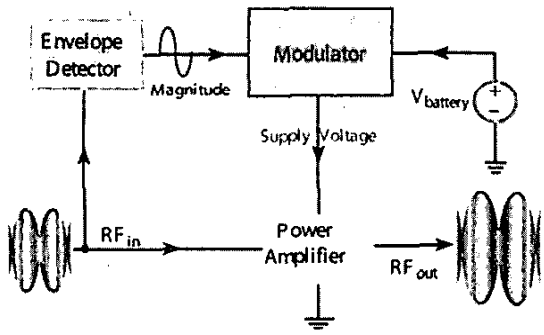

Fig. 2 Envelope following system simplified block diagram.

Envelope following is another technique, where the *PA* supply voltage tracks $A_{in}(t)$, while $v_{in}(t)$ is applied to the input of *PA* [2]. As shown in the simplified block diagram of Fig.2, a detector extracts $A_{in}(t)$ and applies it as a reference signal to the modulator block, which is connected to the battery input voltage. The modulator converts the input DC battery voltage to a time varying DC output voltage proportional to $A_{in}(t)$ to supply the *PA*. The input DC power to the *PA* is the product of its average supply voltage and its supply current. Therefore, for a supply modulated *PA* with a high peak to average power ratio, the average supply voltage is much less than a constant supply voltage, and this results in more efficiency. High efficiency, high bandwidth *DC-DC* converters are required to dynamically vary the battery voltage and supply the *PA*.

High efficiency, small size, low cost, and low noise are the primary requirements of *DC-DC* converters in portable applications. The suitability for monolithic implementation of the three candidates namely, low dropout linear *(LDO)* [3], switched capacitor *(SC)* [4], and switched-mode *(SM) DC-DC* converters is summarized in TABLE I. Considering the high efficiency and high bandwidth requirements, the *(SM) DC-DC* converters are the best option for supply modulation of a *PA*. Their efficiency can ideally approach 100%. The size of passive components can be reduced to practical values for integration by increasing the switching frequencies to the order of 100 MHz [5]. However, the key barrier for monolithic implementation of *SM DC-DC* converters is that the existing monolithic magnetics technology cannot provide high-quality inductors of suitable size.

In this paper we present the results of a monolithic supply modulated *PA*. The system is the main building block of the distributed power supply architecture implemented in a 0.18 μm *SiGe BiCMOS* process technology [6] and shown in Fig. 1. The envelope following system consists of a synchronous buck *SM DC-DC* converter, which is integrated with and supplies a 900 MHz *PA*, while tracking the envelope of the *RF* input signal. A two-stage interleaved synchronous buck converter supplies the digital and analog load on chip.

TABLE I *DC-DC* Converter Topologies.

DC-DC	Advantages	Disadvantages
LDO	• No Magnetics • Simple, Integrable • Low Noise	• Poor Efficiency • Only step-down • Large filter cap.
SC	• No magnetics • Integrable • Step-up, step-down	• Poor Efficiency • High switch count • High noise
SM	• High efficiency • Low switch count • Step-up, step-down	• Monolithic inductor • High noise

II. CIRCUIT OPERATION

Figure 3 shows the circuit diagram of the monolithic envelope following system, where a synchronous buck converter supplies the *RF PA*. A class-AB *PA* is designed to operate in the GSM-900 mobile transmit band with a 25 MHz bandwidth. The *PA* output filter, which consists of parallel connection of inductor L_0 and capacitor C_0 is designed to operate within the desired bandwidth and suppress the higher harmonics. The source impedance R_S is matched to the *PA* input impedance to ensure maximum power delivery, thus maximizing the power added efficiency.

The envelope of the *RF* input signal is applied as signal V_{ref} to the input of the comparator, which compares it with the output voltage of the DC-DC converter, V_{out}, and generates the *PWM* signal. The controller block generates the gate pulses $\varphi_1(t)$ and $\varphi_2(t)$ from the *PWM* signal, to control the switching of MOSFETs M_1 and M_2. If the MOSFETs are assumed as ideal switches in series with on-state resistances R_{on1} and R_{on2}, with series inductor resistance of R_{Lf}, the duty cycle D of the *PWM* signal becomes:

$$D = \frac{I_o(R_{on2} + R_{Lf}) + V_{out}}{I_o(R_{on2} - R_{on1}) + V_{in}} \approx \frac{I_o(R_{on2} + R_{Lf}) + V_{out}}{V_{in}} \quad (3)$$

The values of L_f and C_f, which are interrelated and govern the output voltage ripple of the converter, should be as small as possible for monolithic implementation. In order to overcome the transient limitation of conventional synchronous buck converter, the inductor value is chosen such that the peak-peak inductor current is twice the full load current. As a result the inductor current goes negative in all load range.

$$L_f \le \frac{(V_{in} - V_{out})D}{2 f_S I_o} \quad (4)$$

$$C_f = \frac{1}{8} \frac{1}{\frac{\Delta V_{out}}{V_{out}}} \frac{(1-D)}{f_S^2 L_f} \quad (5)$$

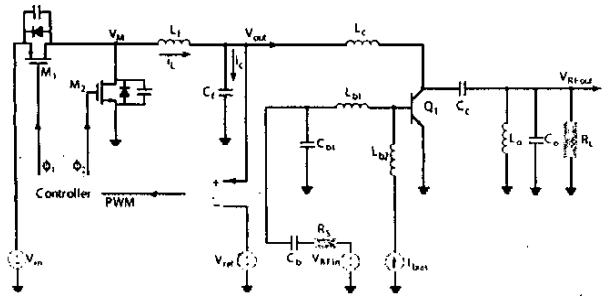

Fig. 3 Monolithic supply modulated RF Power Amplifier.

III. CIRCUIT DESIGN AND IMPLEMENTATION

With high speed, low noise figure (*NF*), excellent linearity, and less dependence of speed upon high field strength and supply voltage, the *SiGe BiCMOS* process is well suited to portable wireless applications. The *IBM Blue Logic™ BiCMOS 6HP* process technology is chosen for fabrication of the monolithic supply modulated *PA* [6]. The deep trench technology provides increased isolation, making this process suitable for mixed-signal designs. Switches M_1 and M_2 are implemented by use of 70A° (3.3V) MOSFETs. NMOS devices are advantageous, but their complex gate drive makes them less attractive for monolithic implementation. Therefore a PMOS device is used for M_1 and the synchronous rectifier M_2 is implemented as an NMOS. The optimum device widths $W_{n,p}$ are obtained by equating the conduction losses and switching losses of the switches to minimize their power loss.

$$W_{n,p} = \frac{i_{rmsn,p}}{C_{ox}V_{in}\sqrt{2.5 f_s \mu_{n,p}(V_{in} - V_t)}} \tag{5}$$

Although metal-to-metal (*MIM*) capacitor option (1.35 fF/μm^2) results in a higher quality factor (Q) and less series resistance [6], but it requires more chip area. Use of stacked *MIM* capacitor option (2.7 fF/μm^2), which unfortunately was not available at the time of design results in a smaller size. In this process, *MOS* capacitors provide higher specific capacitance (3.1 fF/μm^2) but suffer from leakage and non-linearity. The converter filter capacitance C_f is implemented by use of *MOS* option and capacitors C_{b1} and C_c are implemented with *MIM*. The converter efficiency is strongly influenced by the inductor Q, which is limited by metal line resistivity, capacitive coupling to the substrate and magnetic coupling to the substrate. By removing the first few internal turns of the spiral inductor, which do not contribute too much to the total inductance, the effect of metal line resistance is lowered. By use of thick last analog metal layer far above the substrate, the high Q inductors are implemented [6]. Power transistor Q_1 of *PA* is implemented by silicon germanium heterojunction bipolar transistor (*HBT*), which offers high performance of a gallium arsenide (GaAs) device with low power consumption and higher gain and less noise compared to silicon bipolar junction transistor (*BJT*). Although a buck-boost converter topology is desirable to maintain the required supply voltage, while the battery gets depleted, the low breakdown voltage of power MOSFETs and *HBT* justifies the use of a buck converter topology. A 900 MHz *PA* is designed with a 25 MHz bandwidth, the frequency response of which is shown in Fig. 4 at various temperatures. In order to study the effect of process parameter variation, a fixed skew is added to a subset of statistical process parameters set with the variable corner. Independent corners are available for *HBT*, inductor, and capacitor. The effect of process parameter variation on center frequency and bandwidth are shown in Fig. 5.

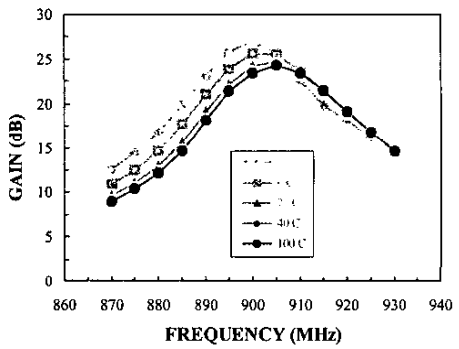

Fig. 4 *PA* frequency response at various temperatures.

Figure 6 compares the power added efficiency of the *PA* with constant and modulated supply voltage. At lower power levels the system with the modulated supply is more efficient because of the ability to optimally control the power supply voltage. As opposed to the *EER* technique, the *PA* remains in class-AB operation and the amplitude of the input signal rather than the supply voltage, controls the amplitude of the output signal. Therefore it is sufficient for the supply voltage to remain in a regime to avoid clipping and increase efficiency and not exactly replicate the input signal.

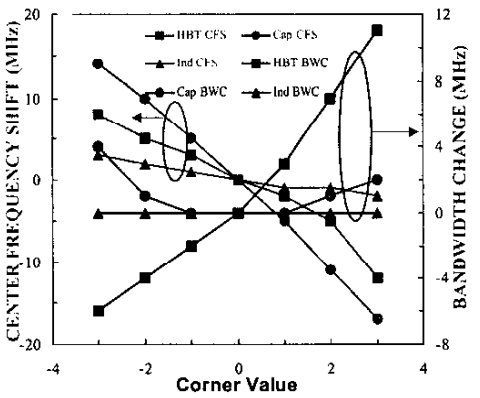

Fig. 5 Statistical process parameter variation results.

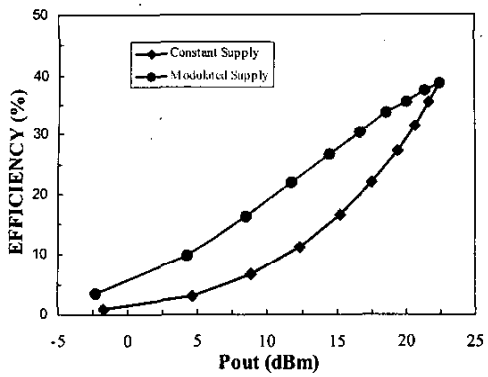

Fig. 6 Variation of efficiency with output power.

A *PWM* synchronous buck converter is implemented with a switching frequency in the order of 100 MHz, which is an order of magnitude higher than the state-of-the-art power converters. High switching frequency results in smaller passives, and allows any sidebands caused by the converter output voltage ripple to be outside the critical frequency bands of interest for most communication standards. Sampling theory requires the switching frequency to be at least twice that of the highest modulation frequency required, although a practical factor of ten is normally considered. An operating frequency of 100 MHz allows for less than 100 ns transient response, which is enough to allow rapid modulation of the supply voltage for many *RF PA* communication purposes. Figure 7 shows the output voltage of the converter and a 10 MHz reference signal input to the converter. The reference and the resulting envelope signal are almost indistinguishable except for the high frequency ripples on the converter output voltage. The layout of the monolithic supply modulated *PA* section of the distributed power supply architecture is highlighted in Fig. 8. C_f, which occupies the majority of space to the right pad frame, is an array of parallel connection of 1 pF unit size cells. M_1 and M_2 are formed by a parallel connection of an array of unit size cells to reduce the RC delay of the gates and ensure uniform distribution of current and gate signals. Thick last layer analog metal is used as low-resistance interconnect between the switches and passive components to reduce distribution losses. The inductors have been implemented by use of the thick analog metal layer far above the substrate.

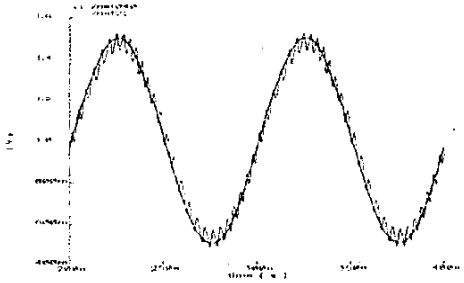

Fig. 7 Tracking simulation result.

IV. CONCLUSION

A monolithic supply modulated *PA* has been designed and implemented by use of a 0.18μm *IBM Blue Logic™ BiCMOS 6HP* process technology for wafer level testing. It consists of a synchronous buck converter and a class-AB *PA*. The results show that a monolithic implementation of the envelope following system can provide a linear *RF PA* with higher efficiency. The converter filter capacitance is implemented by use of MOS capacitor option (1.35 fF/μm^2). The inductors have been implemented by use of the thick analog layer after the 5th layer of metallization and far above the substrate. As passive components process technology continues to mature, the proposed monolithic supply modulated *PA* architecture will meet the stringent size and efficiency requirements of future wireless *SOC* applications.

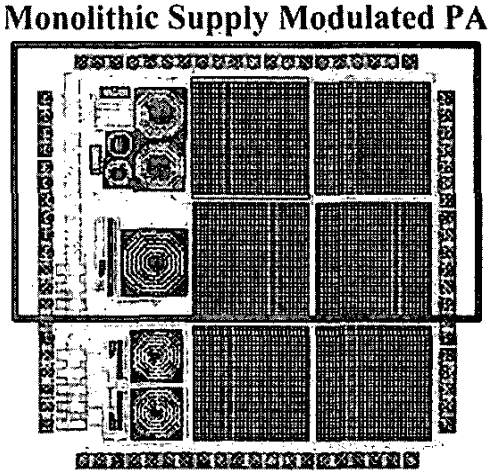

Fig. 8 Monolithic distributed power supply architecture layout.

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